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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,236	01/18/2007	Alessandro Minzoni	I438.111.101	5505

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,236	MINZONI, ALESSANDRO	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/7/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Keeth (5,852,378).

Claim 11, Keeth shows a clock receiver circuit device (50, Fig. 3) comprising:

a first input (56) adapted to be connected with a first connection (CK) of a semi-conductor component (52);

a second input (60) adapted to be connected with a second connection (CK*) of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates (four transfer gates 64, 66, 68, 70).

Claim 12, Keeth shows the receiver circuit device according to claim 11, which comprises four transfer gates (transfer gates 64, 66, 68, 70).

Claims 13 & 14, Keeth shows the receiver circuit device according to claim 11, comprising wherein at a first transfer gate (66) a corresponding first transfer gate control input (88) is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input (80), inverse in relation to the first

transfer gate control input (56 and 60 are inverse), is connected with the first input of the receiver circuit device.

Claim 15, Keeth shows the receiver circuit device according to claim 14, comprising wherein at a second transfer gate (64) connected with the first transfer gate, a corresponding first transfer gate control input (84) is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input (76), inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

Claim 16, Keeth shows the receiver circuit device according to claim 11, comprising wherein at a third transfer gate (70) a corresponding first transfer gate control input (82 is connected to 62 that is 56) is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input (90 is connected to 58 that is 60), inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

Claim 17, Keeth shows the receiver circuit device according to claim 16, comprising wherein at a fourth transfer gate (68) connected with third transfer gate, a corresponding first transfer gate control input (86) is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input (68), inverse in relation to the first transfer gate control input, is connected with first input of the receiver circuit device.

Claim 18, Keeth shows the receiver circuit device according to claim 11, in which differential clock signals (CK is complementary of CK*) are present at the first and second inputs.

Claim 19, Keeth shows a clock receiver circuit device (50, Fig. 3) comprising:

a first input (56) adapted to be connected with a first connection (CK) of a semi-conductor component (52);

a second input (60) adapted to be connected with a second connection (CK*) of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates (four transfer gates 64, 66, 68, 70), and wherein a signal (Vnode A) detectable between a first (66) and second (64) transfer gate and/or a second signal (Vnode B) detectable between a third (70) and fourth (68) transfer gate, is used to boost a clock relaying circuit (100 and 102).

The limitations of claims 20-23 are rejected as above claims 12-17.

Claim 24, Keeth shows a clock receiver circuit device (50, Fig. 3) comprising:

a first clock input (56) for receiving a first clock signal (CK);

a second clock input (60) for receiving a second clock signal (CK*), inversely equal to the first clock signal (CK* is inverse equal to CK);

wherein at a first transfer gate (66) a corresponding first transfer gate control connection (88) is connected with the second clock input of the clock receiver circuit

device, and a corresponding second transfer gate control connection (80), inverse in relation to the first transfer gate control connection, with the first clock input of the clock receiver circuit device; and

wherein at a second transfer gate (64) a corresponding first transfer gate control connection (84) is connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection (76), inverse in relation to the first transfer gate control connection, with the second clock input of the clock receiver circuit device,

wherein corresponding further connections (72) of the transfer gates are connected with each other and are jointly connected with a clock output (Vnode A) for emitting a clock output signal.

Claim 25, Keeth shows a semi-conductor component (Fig. 3) having a receiver comprising:

a clock receiver circuit device (50, Fig. 3) comprising:

a first input (56) adapted to be connected with a first connection (CK) of a semi-conductor component;

a second input (60) adapted to be connected with a second connection (CK*) of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates (64, 66, 68, 70).

The limitations of claims 26-29 are rejected as above claims 12-17.

Claim 30, Keeth shows a clock receiver circuit device (50, Fig. 3) comprising:

a first clock input (56) for receiving a first clock signal (CK);

a second clock input (60) for receiving a second clock signal (CK*), inversely equal to the first clock signal (CK* is inversely equal to CK);

wherein at a first transfer gate (66) a corresponding first transfer gate control connection (88) is connected with the second clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection (80), inverse in relation to the first transfer gate control connection, with the first clock input of the clock receiver circuit device; and

wherein at a second transfer gate (64) a corresponding first transfer gate control connection (84) is connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection (76), inverse in relation to the first transfer gate control connection, with the second clock input of the clock receiver circuit device, wherein corresponding further connections (72) of the transfer gates are connected with each other and are jointly connected with a clock output (Vnode) for emitting a clock output signal.

Claim 30, Keeth shows a clock receiver circuit device (50, Fig. 3) comprising:

means for a first input (56) adapted to be connected with a first connection (CK) of a semi-conductor component;

means for a second input (60) adapted to be connected with a second connection (CK*) of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates (64, 66, 68, 70).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANH Q. TRAN
PRIMARY EXAMINER

11/2/07